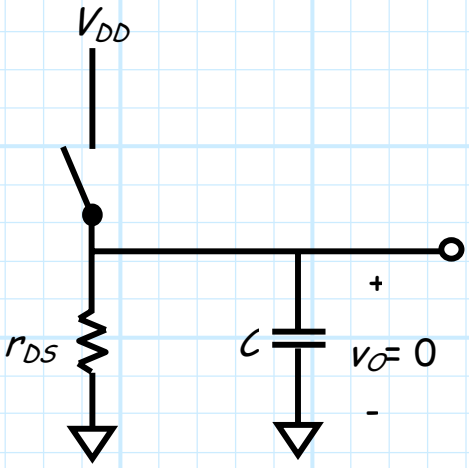
CMOS Propagation Delay

The **CMOS model** can likewise be used to estimate the **propagation delay** of a CMOS inverter.

To see how, consider a CMOS inverter with its **output** at **low** level v_O=0.0 (i.e., its input is v_I=5.0). The voltage across the **output capacitance** C is likewise **zero**:



Q: ***Output capacitance?!*** *What on Earth is that?*

A: The **output capacitance** of a CMOS inverter is simply a value that represents the **total capacitance** associated with the inverter output. This includes the internal capacitances of the MOSFET devices, the wiring capacitance, and the capacitance of the device that the output is connected to!

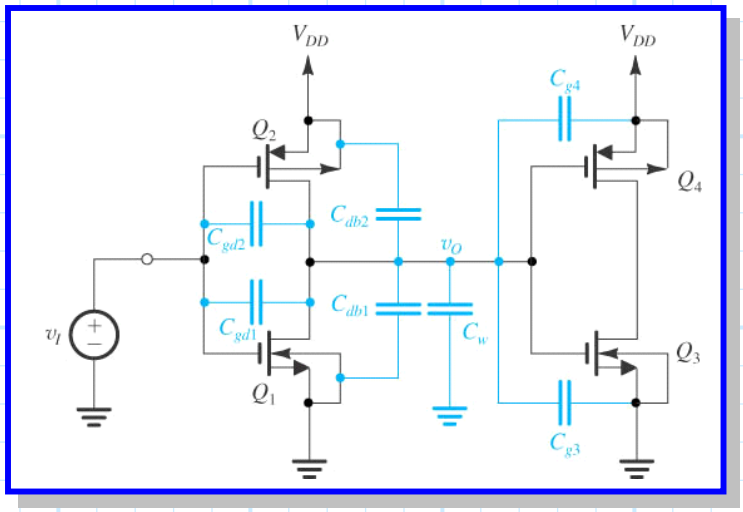


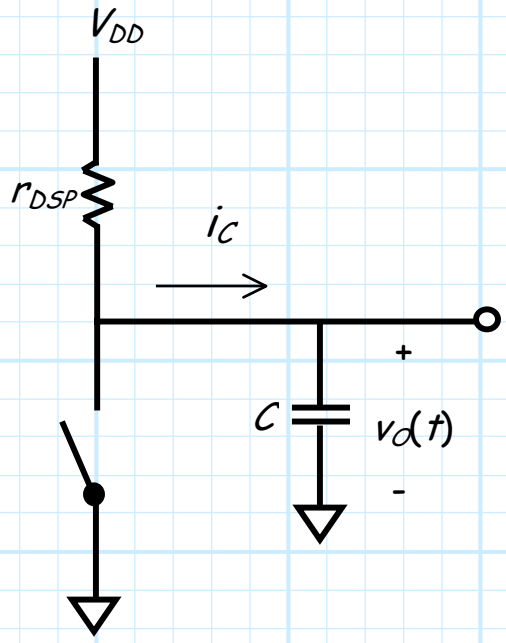
Figure 10.6 (p. 958) – *Schematic showing all capacitances associated with the output of a CMOS inverter.*

Now, say the input of the inverter instantaneously **changes** to a low level v_I=0.0. **Ideally,** the output would likewise **instantaneously** change to a high level $v_O = V_{DD}$. However, **because** of the output capacitance, the output voltage will **not** instantaneously change state, but instead will change "slowly" with time.

Specifically, using the **MOSFET model**, we can determine the output voltage as a **function of time**:

From KCL:

$$\frac{V_{DD} - v_O(t)}{r_{DSP}} = C\frac{dv_O(t)}{dt}$$



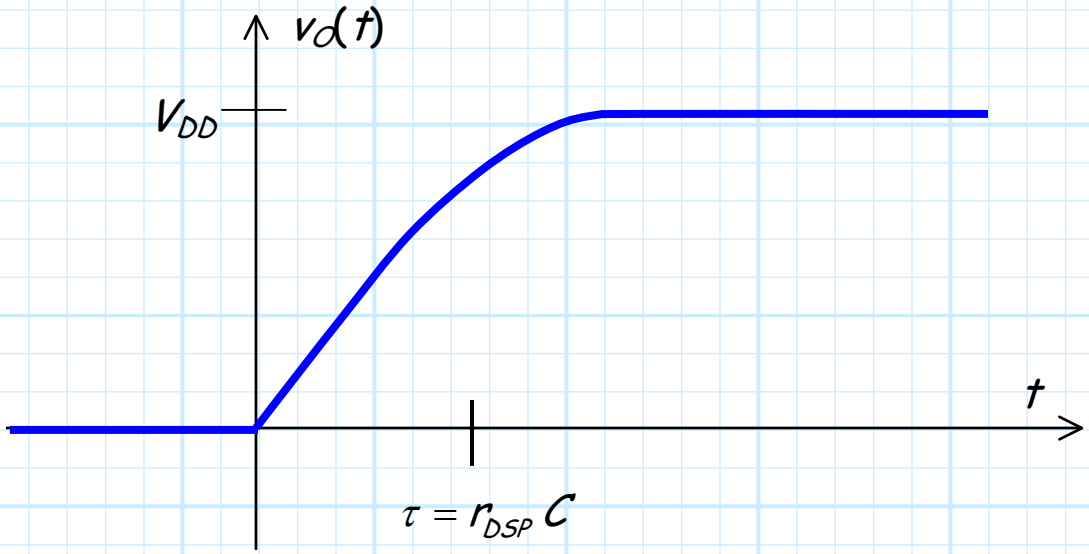
resulting in the **differential equation**:

$$V_{DD} - v_O(t) - r_{DSP}C\frac{dv_O(t)}{dt} = 0$$

Solving this differential equation, using the **initial condition** $v_O(t)$ =0.0, we get:

$$v_O(t) = V_{DD}\left(1 - e^{-t/\tau}\right)$$

where τ is the **time constant** $\tau = r_{DSP}C$.



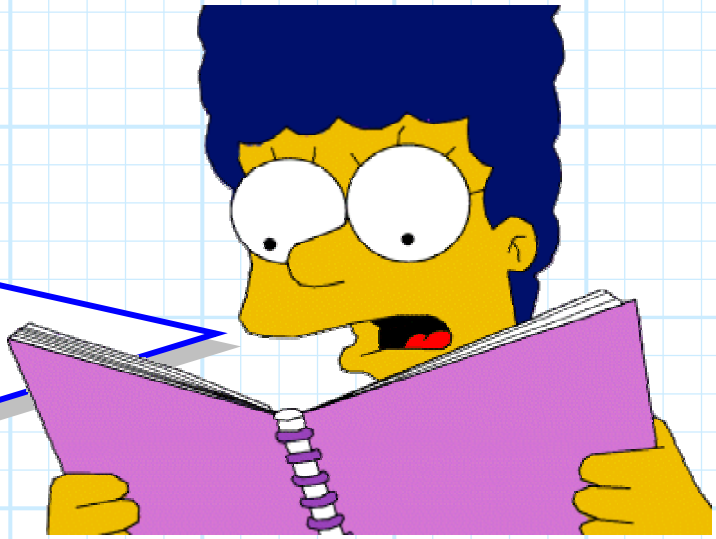
The time constant τ is therefore the approximate time it takes for the output voltage to change after the input has changed. As such, the value τ is **approximately** the **propagation delay** t_p of the CMOS inverter!

$$t_p \approx r_{DSP} C = \frac{C}{2K(V_{DD} - V_t)}$$

Look at what this means! We can **reduce** the propagation delay of a CMOS inverter by either:

1. Increasing K
2. Decreasing V_t
3. Decreasing C

Q: *But wait! Didn't you say earlier that if we increase K or decrease V_t, we will increase* ***peak current*** *i_D^{max}, and thus increase the dynamic* ***power dissipation*** *P_D??*



A: True! That is the dilemma that we face in **all** electronic design—**increasing** the **speed** (i.e., decreasing the propagation delay) typically results in **higher power dissipation**, and vice versa.

Our only option for decreasing the propagation delay **without** increasing the power dissipation is to **decrease the output capacitance** *C*!

Output capacitance *C* can be reduced only by decreasing the **size** of the MOSFET devices—making the devices **smaller** likewise make them **faster**!